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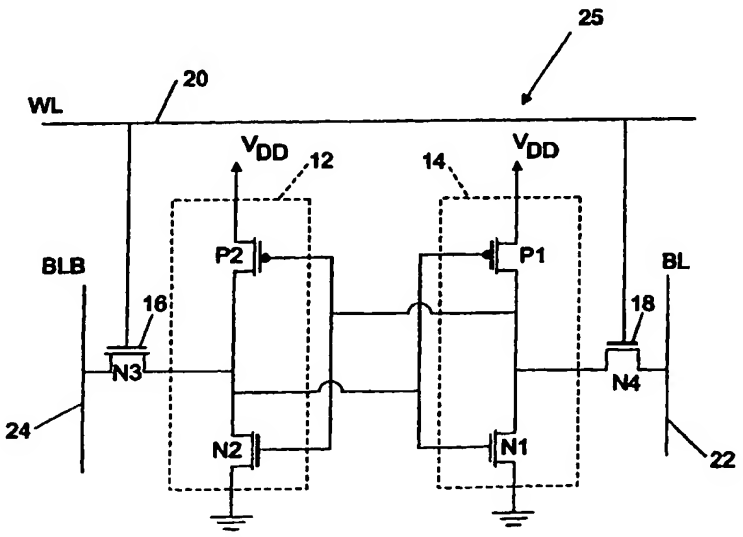
(54) Title: LOW LEAKAGE ASYMMETRIC SRAM CELL DEVICES



(57) Abstract: Asymmetric SRAM cell designs exploiting data storage patterns found in ordinary software programs wherein most of the bits stored are zeroes for data and instruction streams. The asymmetric SRAM cell designs offer lower leakage power with little impact on latency. In asymmetric SRAM cells, selected transistors are "weakened" to reduce leakage current when the cell is storing a zero. Transistor weakening may be achieved by using higher voltage threshold transistors, by varying transistor geometries, or other means. In addition, a novel sense amplifier design is provided that leverages the asymmetric nature of the asymmetric SRAM cells to offer cell read times that are comparable with conventional symmetric SRAM cells. Lastly, cache memory designs are provided that are based on asymmetric SRAM cells offering leakage power reduction while maintaining high performance, comparable noise margins, and stability with respect to conventional cache memories.

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